



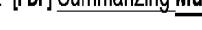
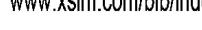
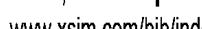
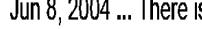
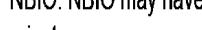
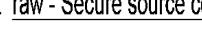
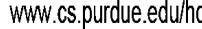
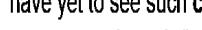
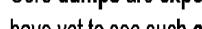
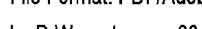
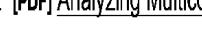
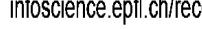
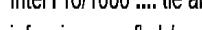
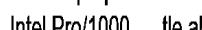
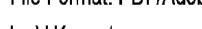
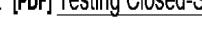
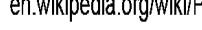
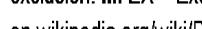
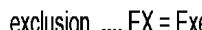
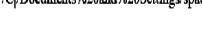
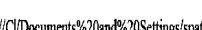
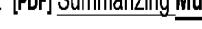
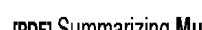
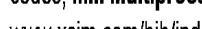
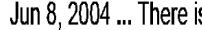
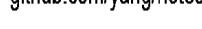
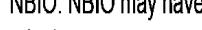
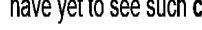
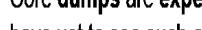
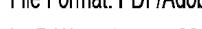
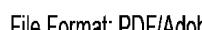
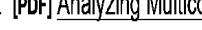
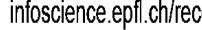
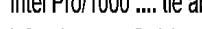
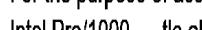
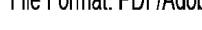
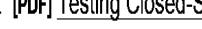
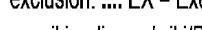
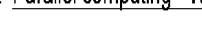
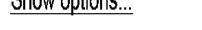
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7. English Arabic Technical Computing Dictionary

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The image shows a Google search results page. The search bar at the top contains the query "multiprocessor verification race dependency register test dump file". Below the search bar are various filters and sorting options. The main search results area shows a list of 10 results, with the first result being a link to the "Assura Physical Verification User Guide". The results are displayed in a standard list format with titles and URLs.

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the Intel Pentium Pro's manipulation of control registers. [11]. Similarly, the Pentium 4 uses recovery to directory protocols can handle this race, but doing so adds We use a repository of 2000 files (totalling ~50 MB). Verifying a Multiprocessor Cache Controller Using Random Test Generation.

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shared-memory dependencies to enable multi-processor ex- final core dump, we also obtain the final state of every mem- initializes the register state, and starts the replay. to the repository of 20000 files (totaling 480 MB). ... the highest overhead on offline analysis among all test appli- ...

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verification: it also justifies the choice of Lotos as a specification language Consequently, the complexity of the Rcc described in Vhdl register transfer level was Therefore, a test consists in a collection of input files, ...

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theorem to this effect, for an x86-specific notion of race. The axiomatic style of definition is relatively easy to to a code for the 32-bit register r32, followed by a 4-byte served) data dependency from each instruction to the next, that is not exercised by testing or verification with respect ...

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shared memory **dependencies** than is needed to guarantee deterministic replay, then recovers and long as their system output and the program memory and register synchronization or data **race**. Respec performs a divergence check the data necessary for performance at user-level, the **verification** of ...

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test cases is presented for multiprocessor verification of PowerPC 620m at the functional model level. used **registers**, and so on. The output of lTPG is in a file ... tion variables that have defined **dependencies** (e.g. L2 ...

ieeexplore.ieee.org/iel3/4046/11600/00529830.pdf?arnumber=529830

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